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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,123	08/04/2003	Edmund Koon Tian Lua	2269-5709US (02-1462.00/U)	5763
24247	7590	03/14/2005	EXAMINER	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			ANDUJAR, LEONARDO	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/634,123	LUA ET AL.
	Examiner Leonardo Andújar	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 22 February 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-46 is/are pending in the application.
- 4a) Of the above claim(s) 1-25 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 26,27,30-38 and 40 is/are rejected.
- 7) Claim(s) 28,29,39 and 41-46 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 04 August 2003 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>08/03 and 9/03</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of group II (claims 26-46) in the reply filed on 03/01/2005 is acknowledged.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 26, 27, 30, 32, 36, 38 and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Yew et al. (US 6,049,129).

5. Regarding claim 26, Yew (e.g. figs. 2 & 3) shows a semiconductor assembly comprising: at least one semiconductor die having a plurality of bond pads 120 formed on active surface thereof; at least one anisotropically conductive layer 70 comprising a plurality of laterally isolated conductive elements 84 disposed in a dielectric material 72 (i.e. FR-4) and having an upper end exposed therethrough attached to the active surface by the adhesive layer 60; a plurality of conductive bumps 150 on the at least one anisotropically conductive layer with each of eh plurality of conductive bumps in

contact with at least one conductive element of the plurality; and wire bonds 80 between the bond pads and the conductive bumps.

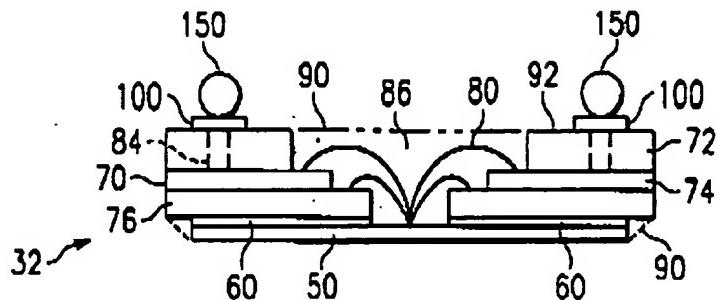


FIG. 3

6. Regarding claim 27, Yew shows that the anisotropically conductive layer comprises conductive elements in the form of discrete metal columns embedded in a polymeric material.

7. Regarding claim, 30 Yew shows that the polymeric material comprises a film.

8. Regarding claim 32, Yew discloses that the anisotropically conductive layer is attached to the active surface by an adhesive 60 (col. 3/lls. 47-68).

9. Regarding claim 36, Yew discloses that the conductive bumps are attached to the conductive element by metallurgical bonds (col. 5/lls. 21-25). Note that a metallurgical bond is formed when a solder bump is attached to the pad by solder reflow.

10. Regarding claim 38, Yew teaches that the semiconductor die has a plurality of bond pads centrally located along an axis thereof and the anisotropically conductive layer comprises a plurality of anisotropically conductive layers adjacent the plurality of bond pads on opposing sides thereof (e.g. fig. 2).

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11. Regarding claim 40, Yew teaches that the semiconductor die is in the form of singulated die.

Claim Rejections - 35 USC § 103

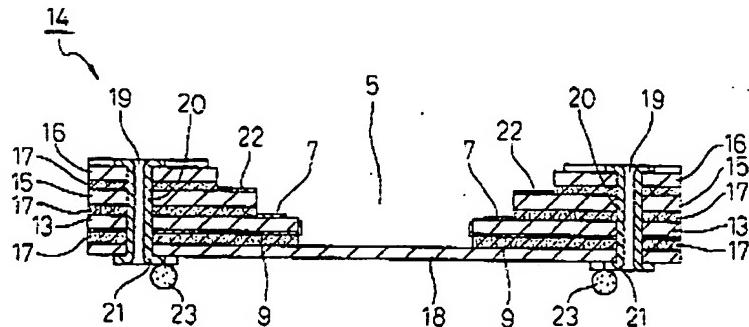
12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. (US 6,049,129) in view of Sato (US 5,858,816).

14. Regarding claim 31, Yews shows most aspect of the instant invention except for a conductive element comprising at least one of tungsten, aluminum, copper, silver, gold, and alloys thereof. Nevertheless, Sato (e.g. fig. 3) shows a structure analogous to the conductive layer 72 disclosed by Yews were the conductive element 20 is made of copper.

Fig.3

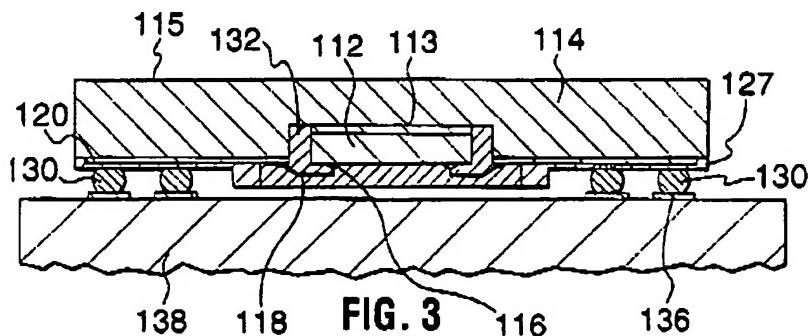


It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the conductive element disclosed by Yew of copper as

suggested by Sato because copper has a high conductivity, is easily fabricated, and has an excellent corrosion resistance in natural environments.

15. Claims 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. (US 6,049,129) in view of Marcantonio (US 5,796,170).

16. Regarding claim 33, Yew teaches most aspects of the instant invention including semiconductor substrate assembly attached to a substrate (col. 2/29-32). Yew does not disclose a substrate having a plurality of terminal pads on a surface thereof; and wire bonds between the plurality of conductive bumps and the plurality of terminal pads. Nevertheless, Marcantonio (e.g. fig. 3) teaches an analogous embodiment that includes a substrate 138 having a plurality of terminal pads 136 on a surface thereof, and wire bonds 118 between the plurality of conductive bumps and the plurality of terminal pads. This type of substrate serves a variety of functions. Foremost, it contains the wiring required to interconnect the components electrically, acts as the primary structure to supports those components and is also used to conduct away heat generated by the components.



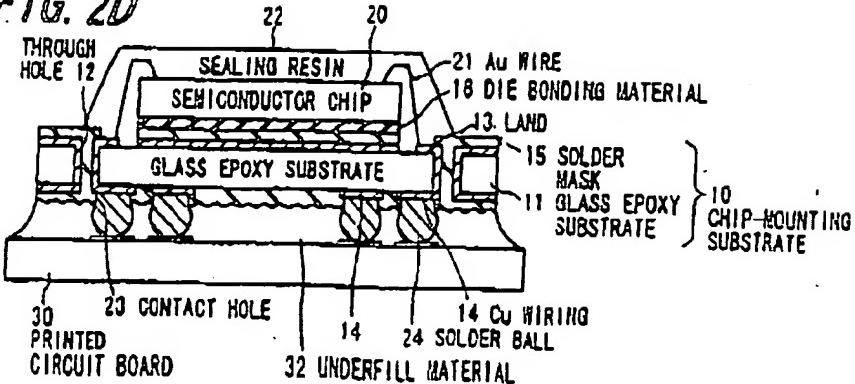
It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a substrate having a plurality of terminal pads on a

surface thereof in Yew's invention as suggested by Marcantonio to provide support, a interconnection medium and a heat transfer path. Note that in this combination the wire bonds are located between the plurality of conductive bumps and the plurality of terminal pads.

17. Regarding claim 34, Marcantonio shows that the substrate comprises a circuit board (e.g. fig. 4).

18. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. (US 6,049,129) in view of Kobayashi (US 6,806,560).

19. Regarding claim 35, Yew teaches most aspects of the instant invention including semiconductor substrate assembly attached to a substrate (col. 2/29-32). Also, Yew shows a dielectric layer 86 over the at least one semiconductor die, the bond pads and the wire pads. Yew does not teach that the dielectric layer is extended to cover the conductive bumps. Nevertheless, Kobayashi (e.g. fig. 2D) teaches a dielectric layer 32 at the outer surface of a dielectric layer 41 and covering conductive bumps 24. According to Kobayashi, this type of embodiment absorbs a stress caused by a difference in the thermal expansion coefficient between the die mounting structure and the substrate and impacts caused by fallings to secure the reliability of soldered jointed portions (col. 1/lls. 34-41).

FIG. 2D

It would have been obvious to one of ordinary skill in the art at the time the invention was made to cover the outer surface and the conductive bumps disclosed by Yew in order to absorb a stress caused by a difference in the thermal expansion coefficient between the die mounting structure and a substrate and impacts caused by fallings to secure the reliability of soldered jointed portions as suggest by Kobayashi.

20. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. (US 6,049,129) in view of Wu (US 6,727,579).

21. Regarding claim 37, Yew discloses that the wire bonds are made of gold (col. 6/lls. 60-64). Yew does not disclose that the conductive bumps are made of gold. Nevertheless, Wu teaches that gold is a suitable material for making conductive bumps (col. 3/lls. 21-23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the conductive bump disclosed by Yew of gold as suggested by Wu because gold is highly resistant to many corrosive environments, is tarnish resistant, is highly resistant to spark erosion and because of its thermoelectric stability.

Allowable Subject Matter

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22. Claims 28, 29, 39 and 41-46 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Leonardo Andújar
Patent Examiner
Art Unit 2826
03/02/2005